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# Effect of Grain Boundaries on the I-V Electrical Characteristics for Low Temperature Polycrystalline Silicon TFTs: 2D-Numerical Simulations

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**Abstract:**

Recently polycrystalline silicon (pc-Si) thin film transistors (TFTs) have emerged as the devices of choice for many applications such as scanners, image sensors, printers heads, SRAMs, EEPROMs and AMLCDs (Active Matrix Liquid Crystal Displays) where they are being used for the switching of flat panel liquid crystal displays. The TFTs are made of a thin un-doped polycrystalline silicon film deposited on a glass substrate by the Low Pressure Chemical Vapor Deposition technique LPCVD; this choice limits the technological process to the temperature < 600°C.The benefit of pc-Si is to make devices with large grain size. Unfortunately, according to the conditions during deposition, the pc-Si layers can consist of a random superposition of grains of different sizes, where it appears grains boundaries parallels and perpendiculars. In this paper, the transfer characteristics $I_{DS}$-$V_{GS}$ are simulated by solving a set of two-dimensional (2D) drift-diffusion equations; together with the usual density of states (DOS: exponential band tails and Gaussian distribution of dangling bonds) localized at the grains boundaries.
The effects of the position, the number of grains boundaries and grain size on the TFTs characteristics have been also investigated.